ABSTRACT OF THE DISCLOSURE

A accurate time measurement circuit. The design is amenable to implementation as a CMOS integrated circuits, making the circuit suitable for a highly integrated system, such as automatic test equipment where multiple time measurement circuits are required. The circuit uses a delay locked loop to generate a plurality of signals that are delayed in time by an interval D. The signal to be measured is fed to a bank of delay elements, each with a slightly different delay with the difference in delay between the first and the last being more than D. An accurate time measurement is achieved by finding coincidence between one of the TAP signals and one of the delay signals. The circuit has much greater accuracy than a traditional delay line based time measurement circuit with the same number of taps. It therefore provides both accuracy and fast re-fire time and is less susceptible to noise.